WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first circuit comprising an input, an output, a reference terminal, a series pass device connected between the input and the output, and a control circuit operable to (a) sense a series current flowing through the series pass device and (b) control the series pass device;

the control circuit comprising a negative feedback loop to control an average power dissipation in the first circuit by comparing the series current with a signal at the reference terminal.

2. The apparatus of Claim 1, further comprising:

a plurality of first circuits having their respective inputs connected together, having their respective outputs connected together, and having their respective reference terminals connected together;

the control circuits in each of the plurality of first circuits adapted to equally share the power dissipation in each of the plurality of first circuits.

3. The apparatus of Claim 1, wherein the first circuit is a low dropout (LDO) type circuit.

4. The apparatus of Claim 1, wherein the first circuit is operable to linearly regulate voltage at a load by manipulating a resistance placed in series with the load.

5. An apparatus comprising:

a first circuit comprising an input, an output, a reference terminal, a series pass device connected between the input and the output, and a control circuit, the control circuit comprising a negative feedback loop, the control circuit being operable to (a) sense a current flowing through the series pass device and (b) adjust the current flowing through the series pass device.

6. The apparatus of Claim 5, further comprising:

a plurality of first circuits having their respective inputs connected together, having their respective outputs connected together, and having their respective reference terminals connected together;

wherein the control circuit in each first circuit is adapted to adjust the current flowing through the series pass device to be substantially equal to other currents flowing through other series pass devices in other first circuits.

7. The apparatus of Claim 5, in which the control circuit is adapted to decrease power dissipation by decreasing a voltage across the series pass device as the current through the controlled circuit element increases.

8. The apparatus of Claim 5, in which the control circuit is adapted to reduce voltage variations at the output of the series pass device, the voltage variations being present at the input to the series pass device.

9. The apparatus of Claim 5, in which the series pass device comprises a metal oxide semiconductor field effect transistor (MOSFET).

10. The apparatus of Claim 5, wherein the control circuit comprises a first amplifier and a second amplifier, the second amplifier having an output coupled to the series pass device.

11. The apparatus of Claim 10, wherein first and second inputs of the first amplifier are coupled to first and second ends of a resistor, the resistor being in series with a source terminal of the series pass device.

12. The apparatus of Claim 10, wherein an output of the first amplifier is coupled to a resistor and a capacitor, the resistor being coupled to an input of the second amplifier.

13. The apparatus of Claim 10, wherein an output of the first amplifier is coupled to first and second paths, the first path comprising a first resistor and a first capacitor, the second path comprising a second resistor and a second capacitor, the first path being coupled to a first input of the second amplifier, the second path being coupled to a second input of the second amplifier.

14. The apparatus of Claim 13, wherein a time constant of the first resistor and first capacitor is substantially equal to a time constant of the second resistor and second capacitor.

15. A method comprising:

sensing a first current produced by a first filter circuit; and

adjusting the first current to substantially match a second current produced by a second filter circuit which is in parallel with the first filter circuit.

16. The method of Claim 15, further comprising supplying a common load with the first and second currents.

17. The method of Claim 15, further comprising increasing a voltage at a transistor in the first filter circuit when the first current is lower than the second current.

18. The method of Claim 15, further comprising decreasing a voltage at a transistor in the first filter circuit when the first current is higher than the second current.

19. The method of Claim 15, further comprising reducing voltage variations at an output of the first filter circuit, the voltage variations being present at an input to the first filter circuit.

20. An apparatus comprising:

a first controlled circuit element adapted to output a first current; and

a control circuit adapted to (a) sense the first output current from the first controlled circuit element and (b) adjust current through the controlled circuit element when the first output current does not match a second output current of a second controlled circuit element.

21. The apparatus of Claim 20, wherein the first controlled circuit element comprises a metal oxide semiconductor field effect transistor (MOSFET).

22. The apparatus of Claim 20, wherein the control circuit comprises first and second amplifiers, resistors and capacitors.

23. An apparatus comprising:

a circuit adapted to be connected in parallel with a similar circuit, the circuit comprising:

a first amplifier; and

a second amplifier, wherein an output of the first amplifier is coupled to first and second paths, the first path being coupled to a first input of the second amplifier, the second path being coupled to a second input of the second amplifier, wherein the first and second paths act as a feedback path for sensing current through the circuit, wherein the second input of the second amplifier is coupled to a reference terminal in common with one or more parallel circuits.

24. The apparatus of Claim 23 further comprising a series pass device controlled by an output of the second amplifier.

25. A circuit adapted to provide an offset on a non-inverting pin of an amplifier to compensate for differences on the inverting pin, the amplifier providing an active resistance.